IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 15265US01

In the Application of:

Shervin Moloudi et al.

U.S. Serial No.: 09/691,634

Filed: October 18, 2000

For: ADAPTIVE RADIO TRANSCEIVER WITH A POWER AMPLIFIER

Examiner: Marceau Milord

Group Art Unit: 2682

Confirmation No.: 7052

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Michael T. Cruz
Reg. No. 44,636

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is a Brief in support of an Appeal. A Notice of Appeal was received by the United States Patent and Trademark Office on September 2, 2005. A Petition for a One-Month Extension of Time has been enclosed, thereby extending the deadline by which to file an Appeal Brief to December 2, 2005.

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine, California 92618-3616, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment filed with the present application and recorded on Reel 011550, Frame 0086.

RELATED APPEALS AND INTERFERENCES

There are currently no appeals pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-95 are pending in the present application. Pending claims 1-95 have been rejected under 35 U.S.C. § 103(a) and are the subject of this appeal.

STATUS OF THE AMENDMENTS

There are no amendments pending in the present application.

SUMMARY OF THE INVENTION

Some embodiments according to some aspects of the present invention may provide an amplifier that includes, for example, a plurality of differential pairs and a current switch. The plurality of differential pairs may be coupled together through a common differential output. Each differential pair may have a current control input. The current switch may be coupled to the current control input of one of the differential pairs to selectively switch one of the differential pairs in or out of the amplifier.

Some embodiments according to some aspects of the present invention may provide an amplifier that includes, for example, a plurality of amplifying stages and a current switch. The plurality of amplifying stages may each have first and second transistors that may each have first, second and third nodes. The first nodes of the first transistors may be coupled together and the first nodes of the second transistors may be coupled together to form a differential output. The second nodes of the first transistors may be coupled together and the second nodes of the second transistors may be coupled together to form a differential input. The third node of each of the first transistors may be coupled to the third node of its respective second transistor to form a current control input for each of the amplifying stages. The current switch may be coupled to the current control input of one the amplifying stage to switch one of the amplifying stages in or out of the amplifier.

Some embodiments according to some aspects of the present invention may provide an amplifier that may include, for example, a plurality of amplifying stages and a current switch. The plurality of amplifying stages may be coupled together. Each of the amplifying stages may have a current control input. The current switch may be coupled to the current control input of one of the amplifying stages to selectively switch one of the amplifying stages in or out of the circuit.

Some embodiments according to some aspects of the present invention may provide an amplifier that may include, for example, a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level.

Some embodiments according to some aspects of the present invention may provide an amplifier may include, for example, a plurality of amplifying states, switching means and matching means. The plurality of amplifying stages may be coupled together. The switching means may switch one of the amplifying stages in or out of the amplifier to program power of the amplifier. The matching means may match a load coupled to an output of the amplifier. The matching means may be substantially independent of the programmed power.

ISSUES FOR REVIEW

Whether claims 1-18, 20-38, 40-59 and 61-94 are unpatentable under 35 U.S.C. § 103(a) as being obvious over United States Patent No. 6,194,962 B1 to Marcellus R. Chen ("Chen") in view of United States Patent No. 4,901,030 to Stephen P. Webster ("Webster").

Whether claims 19, 39, 60 and 95 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster and further in view of United States Patent No. 6,175,279 B1 to Steven C. Ciccarelli et al. ("Ciccarelli").

GROUPING OF CLAIMS

Claims 1-95 do not stand or fall together.

Group I. Claims 1-21 stand or fall together.

Group II. Claims 22-41 stand or fall together.

Group III. Claims 42-62 stand or fall together.

Group IV. Claims 63-79 stand or fall together.

Group V. Claims 80-95 stand or fall together.

ARGUMENT

I. Group I: Claims 1-21

Claims 1-18, 20 and 21 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 19 stands rejected under 35 U.S.C. § 103(a) as

being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

Appellants respectfully submit that Chen and Webster were improperly combined.

M.P.E.P. § 2145(X)(D)(2) states that "[i]t is improper to combine references where the references teach away from their combination" (citing, e.g., In re Grasselli, 713 F. 2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983)).

In the SUMMARY OF THE INVENTION section of Chen, Chen teaches "[a] system for adaptively trimming the input offset voltage of an op amp ... which overcomes the problems noted [in the BACKGROUND OF THE INVENTION section]". Chen at col. 2, lines 34-36. The pertinent problem in the prior art according to Chen is that rail-to-rail op amps "typically employ complementary differential pairs, instead of the single differential pair found in conventional amplifiers". Chen at col. 1, lines 23-26. "[B]oth differential pairs contribute to the amplifier's offset voltage [V_{os}] .... Unfortunately, V_{os} will change when one or the other of the pairs stop conducting near the supply rail. When this occurs, the trim adjustment made to correct V_{os} when both pairs are active is now incorrect, and V_{os} will increase". Chen at col. 1, lines 56-63. Thus, teachings of Chen are applicable when "[t]he system is used with an op amp having complementary differential pairs in its input stage, which are typically provided to give the op amp a rail-to-rail common-mode input voltage range". Chen at col. 2, lines 40-43 of the SUMMARY OF THE INVENTION section. "The adaptive trimming system is advantageously employed as long as an op amp includes complementary differential pairs in its input stage". Chen at col. 4, lines 59-62.

On the other hand, Webster teaches that "[t]he improved operational amplifier stages are an input, a gain and an output stage". Webster at the Abstract. Webster describes an input stage 601 that includes a *single* pair of transistors Q101, Q102 that are differentially connected. See, e.g., Webster at FIG. 1; and col. 3, lines 37-40. Thus, Webster only teaches a single pair of differential transistors Q101, Q102 in the input

stage 601 and teaches away from "an op amp having complementary differential pairs in its input stage" as taught by Chen. See, e.g., Chen at col. 2, lines 40-43. The system of Chen would not be applicable to the *single* pair of differential transistors Q101, Q102 of the Webster input stage 601 since Chen is solving the problem relating to trimming voltages V_{os} occurring from *two* complementary differential *pairs* as explained above.

Furthermore, the teachings of Chen relate to rail-to-rail op amps which "typically employ complementary differential pairs, instead of the single differential pair found in conventional amplifiers". Chen at col. 1, lines 24-26. Thus, Chen disparages the operational amplifier of Webster as being merely a conventional amplifier.

In addition, Webster does not appear to be a rail-to-rail op amp further teaching away from the combination of Webster and Chen. Chen teaches a system for use with an op amp with "a rail-to-rail common-mode input voltage range" (Chen at col. 2, lines 42-43) in which the op amp "function[s] for input signals that vary up to the amplifier's positive and negative supply voltages" (Chen at col. 1, lines 21-31). On the other hand, Webster does not appear to teach a rail-to-rail op amp. In fact, Webster teaches away from Chen by teaching that "[t]he input stage is operable within a range of differential voltage signals, the range including common mode voltage signals at or beyond the negative supply supply rail." Webster at the Abstract. Webster states "that the common mode input voltage range can include voltages of almost a V_{be} below the negative supply rail 7". Webster at col. 7, line 68 to col. 8, line 2. Thus, Webster appears to teach away from a rail-to-rail op amp of Chen and appears to teach away from an input stage having two complementary differential transistor pairs as taught by Chen.

Appellants respectfully submit that Chen and Webster were improperly combined since Chen and Webster teach away from each other. Appellants would even go a step further by suggesting that, since the teachings of Chen are used with "an op amp having complementary differential pairs in its input stage, which are typically provided to give the op amp a rail-to-rail common-mode input voltage range", the teachings of Chen would not be applied to the teachings of Webster. Accordingly, Appellants respectfully

submit that there appears to be no suggestion to combine the teachings of Chen and Webster other than impermissible hindsight based on the recited claim elements.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 1 and its rejected dependent claims (i.e., claims 2-21).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 1. Claim 1 recites, for example, "a plurality of differential pairs coupled together though a common differential output".

The Examiner admits that Chen does not teach at least a plurality of differential pairs coupled together through a common differential output. See, e.g., Office Action Made Final of June 29, 2005 at page 2. However, the Examiner offers the teachings of Webster to make up for the teaching deficiencies of Chen. In the Office Action Made Final at page 3, the Examiner is unable to explain where the recited claim elements are in Webster. Instead, the Examiner cites volumes of text: Webster at col. 1, line 41 to col. 2, lines 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52. See Office Action Made Final at page 3.

Webster at col. 1, line 41 to col. 2, line 42 is nothing less than the entire SUMMARY OF THE INVENTION section. The SUMMARY section is broken down to the three main parts of an operational amplifier: an input stage 601, a gain stage 603, and an output stage 605 as illustrated as dashed blocks in FIG. 1 of Webster. Appellants respectfully draw the attention of the Board to FIG. 1 to which the SUMMARY section effectively describes. FIG. 1 of Webster shows the input stage 601, the gain stage 603, the output stage 605 and the bias circuit 607. It is clear that FIG. 1 only shows a single differential pair consisting of transistors Q101, Q102. FIG. 1 does not show "a plurality of differential pairs". Furthermore, the output (i.e., the collector) of transistor Q101 is

connected to the emitter of transistor Q2 and the output (i.e., the collector) of transistor Q102 is connected to the emitter of transistor Q1. Thus, not only does Webster not teach "a plurality of differential pairs", but Webster also does not teach "a plurality of differential pairs coupled together through a common differential output".

Webster at col. 6, line 62 to col. 7, line 66 relates to FIGS. 1 and 4 of Webster. Appellants have already established that FIG. 1 does not teach "a plurality of differential pairs coupled together through a common differential output". Appellants draw the attention of the Board to FIG. 4 of Webster. FIG. 4 shows a schematic of the input stage 601 and part of the bias circuit 607 and part of the gain stage 603. As with FIG. 1, FIG. 4 only shows a single differential pair consisting of the same transistors described above, namely, transistors Q101, Q102. Thus, for the reasons above, not only does FIG. 4 not show "a plurality of differential pairs", FIG. 4 does not show "a plurality of differential pairs coupled together through a common differential output".

Webster at col. 12, lines 15-52 relates to a Darlington pair of transistors. In particular, the Darlington pair of transistors QD, Q9 is illustrated in FIGS. 11 and 12. Appellants respectfully submit that a Darlington pair is not a differential pair of transistors. Appellants respectfully draw the attention to transistors QD, Q9 in FIG. 11 which show that configuration is not a differential pair configuration. FIG. 12 shows another embodiment of transistor QD. Transistor QD, in FIG. 12, comprises current mirror transistors Q104A, Q104B, transistor Q8, resistor R4 and transistor Q105. Appellants respectfully submit that FIGS. 11 and 12 of Webster do not show any differential pairs and thus do not show "a plurality of differential pairs". Furthermore, FIGS. 11 and 12 of Webster do not show "a plurality of differential pairs coupled together through a common differential output".

Having analyzed all the text in Webster cited by the Examiner in support of the obviousness rejection, it appears that Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52 and any and all the figures associated with the cited text do not teach "a plurality of differential pairs" and, in particular, the

cited text and accompanying figures of Webster do not teach "a plurality of differential pairs coupled together through a common differential output".

In the Response to Arguments section of the Office Action Made Final, the Examiner declares that "Applicant's arguments filed on 3-4-2005 have been fully considered by they are not persuasive". The Examiner further declares that FIG. 1 and 2 show "a balanced type differential type amplifier circuit that comprises a mutual conductance differential amplifier circuit having two differential output terminals, a constant-current circuit and a detector (col. 1, lines 43-54; col. 1, line 64 - col. 2, line 10). It is considered that this balance type differential amplifier can be constituted a plurality of differential pairs".

Appellants respectfully draw the attention of the Board to the arguments and rebuttal evidence as set forth above in support of Appellants' conclusion that Webster does not teach "a plurality of differential pairs coupled together through a common differential output". Appellants respectfully draw the attention of the Board to FIG. 1 and, in particular, to the input stage 601 which has a single pair of differential transistors Q101, Q102 and not a plurality of differential transistors. Multiple differential pairs are not taught by the input stage 601 of Webster. Furthermore, no common differential output is shown in FIG. 1. The Examiner alleged "two differential output terminals" in the Office Action Made Final at page 20; however, Webster shows no such output terminals. At the most, Webster shows a single-ended amplifier output at, for example, output 15 of transistor Q9.

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 1. Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 1 and its rejected dependent claims (i.e., claims 2-21).

II. Group II: Claims 22-41

Claims 22-38, 40 and 41 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 39 stands rejected under 35 U.S.C. § 103(a) as being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 22-41.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 22 and its rejected dependent claims (i.e., claims 23-41).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 22. Claim 22 recites, for example, "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output".

The Examiner admits that Chen does not teach at least first nodes of first transistors being coupled together and first nodes of second transistors being coupled together to form a differential output. See, e.g., Office Action Made Final of June 29, 2005 at page 7. However, the Examiner offers the teachings of Webster to make up for the teaching deficiencies of Chen. In the Office Action Made Final at page 7, the Examiner is unable to explain where the recited claim elements are in Webster. Instead, the Examiner cites volumes of text: Webster at col. 1, line 41 to col. 2, lines 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52. See Office Action Made Final at page 7.

Webster at col. 1, line 41 to col. 2, line 42 is nothing less than the entire SUMMARY OF THE INVENTION section. The SUMMARY section is broken down to the three main parts of an operational amplifier: an input stage 601, a gain stage 603, and an output stage 605 as illustrated as dashed blocks in FIG. 1 of Webster. Appellants respectfully draw the attention of the Board to FIG. 1 to which the SUMMARY section effectively describes. FIG. 1 of Webster shows the input stage 601, the gain stage 603, the output stage 605 and the bias circuit 607. It is clear that FIG. 1 only shows a single differential pair consisting of transistors Q101, Q102. FIG. 1 does not show "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set froth in claim 22. The output (i.e., the collector) of transistor Q101 is connected to the emitter of transistor Q2 and the output (i.e., the collector) of transistor Q102 is connected to the emitter of transistor Q1. Thus, Webster not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

Webster at col. 6, line 62 to col. 7, line 66 relates to FIGS. 1 and 4 of Webster. Appellants have already established that FIG. 1 does not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22. Appellants respectfully draw the attention of the Board to FIG. 4 of Webster. FIG. 4 shows a schematic of the input stage 601 and part of the bias circuit 607 and part of the gain stage 603. FIG. 4 does not show "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

Webster at col. 12, lines 15-52 relates to a Darlington pair of transistors. In particular, the Darlington pair of transistors QD, Q9 is illustrated in FIGS. 11 and 12. FIG. 12 shows another embodiment of transistor QD. Transistor QD, in FIG. 12, comprises current mirror transistors Q104A, Q104B, transistor Q8, resistor R4 and transistor Q105. Appellants respectfully submit that FIGS. 11 and 12 of Webster do not show "the first nodes of the first transistors being coupled together and the first nodes of

the second transistors being coupled together to form a differential output" as set forth in claim 22.

Having analyzed all the text in Webster cited by the Examiner in support of the obviousness rejection, it appears that Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52 and any and all the figures associated with the cited text do not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

In the Response to Arguments section of the Office Action Made Final, the Examiner declares that "Applicant's arguments filed on 3-4-2005 have been fully considered by they are not persuasive". The Examiner further declares that FIG. 1 and 2 show "a balanced type differential type amplifier circuit that comprises a mutual conductance differential amplifier circuit having two differential output terminals, a constant-current circuit and a detector (col. 1, lines 43-54; col. 1, line 64 - col. 2, line 10). It is considered that this balance type differential amplifier can be constituted a plurality of differential pairs".

Appellants respectfully draw the attention of the Board to the arguments and rebuttal evidence as set forth above in support of Appellants' conclusion that Webster does not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 22. Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 22 and its rejected dependent claims (i.e., claims 23-41).

III. Group III: Claims 42-62

Claims 42-59, 61 and 62 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 60 stands rejected under 35 U.S.C. § 103(a) as being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 42-62.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 42 and its rejected dependent claims (i.e., claims 43-62).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 42.

The Examiner admits that Chen does not teach at least "a current switch coupled to the current control input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit". To make up for the teaching deficiencies of Chen, the Examiner further alleges that Webster teaches at least these elements. To support this assertion, the Examiner cites the same text as before with respect to the rejection of claims 1 and 22, namely, Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52. Appellants respectfully submit that the cited text and corresponding figures in Webster do not teach *selectively* switching an amplifying stage of a plurality of amplifying stages in or out of a circuit. Furthermore, Webster does not teach "a current switch coupled to the current control

input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit" as set forth in claim 42.

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 42. Accordingly, Appellants have successfully traversed the obviousness rejection with respect to claim 42 and its dependent claims (i.e., claims 43-62).

IV. Group IV: Claims 63-79

Claims 63-79 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 63-79.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 63 and its rejected dependent claims (i.e., claims 63-79).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 63. Claim 63 recites, for example, "a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level". The Examiner maintains that these elements are illustrated in Chen at FIGS. 3 and 4 and described in Chen at col. 2, lines 41-61; col. 3, lines 38-57; and col. 5, lines 3-32. Appellants have carefully reviewed the cited portions

of Chen and cannot find support for a digitally programmable power level and a matching circuit and, in particular, a matching circuit that is substantially independent of the programmed power level. For at least the above reasons, Chen in view of Webster does not render obvious the subject matter recited in claim 63 and its rejected dependent claims (i.e., claims 64-79).

Since Webster does not make up for the teaching deficiencies of Chen and the Examiner makes no such allegation or *prima facie* case in the Office Action Made Final, Chen in view of Webster does not teach each and every element as set forth in claim 63.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 63 and its dependent claims (i.e., claims 64-79).

V. Group V: Claims 80-95

Claims 80-94 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 95 stands rejected under 35 U.S.C. § 103(a) as being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 80-95.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 80 and its rejected dependent claims (i.e., claims 81-95).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For

example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 80. Claim 80 recites, for example, "matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power".

Neither Chen nor Webster, individually or combined, teaches each and every element as set forth in claim 80. For example, claim 80 recites "matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power". Since there is no mention of the load coupled to the output stage 34 of the op amp, Chen does not teach any type of matching with respect to such a load. Instead, Chen is merely concerned with trimming an op amp offset voltage. On the other hand, Webster does not teach at least matching means for matching a load coupled to an output of the amplifier. Webster is silent as to matching a load. Since Webster does not make up for the teaching deficiencies of Chen and the Examiner makes no such allegation or *prima facie* case in the Office Action Made Final, Chen in view of Webster does not teach each and every element as set forth in claim 63. For at least the above reasons, neither Chen nor Webster, individually or combined, renders obvious the subject matter recited in claim 80 and its rejected dependent claims (i.e., claims 81-95).

Accordingly, it is respectfully requested that the Board reverse the obviousness rejection with respect to claim 80 and its rejected dependent claims (i.e., claims 81-95).

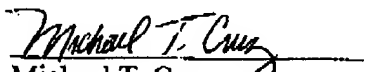
VI. Conclusion

For the foregoing reasons, claims 1-95 are distinguishable over the prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: December 2, 2005

Respectfully submitted,



Michael T. Cruz
Registration No. 44,636
Attorney for Appellants

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8084
Facsimile: (312) 775-8100

APPENDIX

The following claims are involved in this appeal:

1. An amplifier, comprising:

a plurality of differential pairs coupled together through a common differential output, each differential pair having a current control input; and

a current switch coupled to the current control input of one of the differential pairs to selectively switch said one of the differential pairs in or out of the amplifier.

2. The amplifier of claim 1 wherein the differential pairs each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

3. The amplifier of claim 2 wherein the transistors each comprises a field effect transistor

4. The amplifier of claim 3 wherein the first and second transistors in each differential pair each comprises a source coupled to its respective common node.

5. The amplifier of claim 4 wherein the first and second transistors in each of the differential pairs each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

6. The amplifier of claim 3 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form the differential output.

7. The amplifier of claim 1 wherein the current switch comprises a transistor.

8 The amplifier of claim 7 wherein the transistor comprises a field effect transistor.

9. The amplifier of claim 8 wherein the transistor comprises a drain coupled to its respective current control input.

10. The amplifier of claim 1 wherein the current switch comprises a current source having a switch control input.

11. The amplifier of claim 10 further comprising a bias circuit coupled to the switch control input.

12. The amplifier of claim 11 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

13. The amplifier of claim 12 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

14. The amplifier of claim 13 wherein the summer comprises a cascode current mirror.

15. The amplifier of claim 12 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

16. The amplifier of claim 1 further comprising a matching circuit coupled to the common differential output.

17. The amplifier of claim 16 wherein the matching circuit converts a differential current from the common differential output to a single-ended current.

18. The amplifier of claim 16 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the differential pairs is switched in or out of the amplifier.

19. The amplifier of claim 16 wherein the common differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

20. The amplifier of claim 1 wherein the differential pairs are further coupled together through a common differential input, the amplifier further comprising an input stage coupled to the common differential input.

21. The amplifier of claim 1 further comprising a plurality of current switches each coupled to the current control input for a different one of the differential pairs to selectively switch its respective differential pair in or out of the amplifier.

22. An amplifier, comprising:

a plurality of amplifying stages each having first and second transistors, the first and second transistors each having first, second and third nodes, the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output, the second nodes of the first transistors being coupled together and the second nodes of the second transistors being coupled together to form a differential input, and the third node of each of the first transistors being coupled to the third node of its respective second transistor to form a current control input for each of the amplifying stages; and

a current switch coupled to the current control input of one the amplifying stage to switch said one of the amplifying stages in or out of the amplifier.

23. The amplifier of claim 22 wherein the transistors each comprises a field effect transistor.

24. The amplifier of claim 23 wherein the third nodes each comprises a source.

25. The amplifier of claim 24 wherein the second nodes each comprises a gate.

26. The amplifier of claim 23 wherein the first nodes each comprises a drain.

27. The amplifier of claim 22 wherein the current switch comprises a transistor.

28. The amplifier of claim 27 wherein the transistor comprises a field effect transistor.

29. The amplifier of claim 28 wherein the transistor comprises a drain coupled to its respective current control input.

30. The amplifier of claim 22 wherein the current switch comprises a current source having a switch control input.

31. The amplifier of claim 30 further comprising a bias circuit coupled to the switch control input.

32. The amplifier of claim 31 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied the switch control input.

33. The amplifier of claim 32 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

34. The amplifier of claim 33 wherein the summer comprises a cascode current mirror.

35. The amplifier of claim 34 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

36. The amplifier of claim 22 further comprising a matching circuit coupled to the differential output.

37. The amplifier of claim 36 wherein the matching circuit converts a differential current from the differential output to a single-ended current.

38. The amplifier of claim 36 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the amplifying stages is switched in or out of the circuit.

39. The amplifier of claim 36 wherein the common differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

40. The amplifier of claim 22 further comprising an input stage coupled to the differential input.

41. The amplifier of claim 22 further comprising a plurality of current switches each coupled the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

42. An amplifier, comprising:

a plurality of amplifying stages coupled together, each of the amplifying stages having a current control input; and

a current switch coupled to the current control input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit.

43. The amplifier of claim 42 wherein the amplifying stages each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

44. The amplifier of claim 43 wherein the transistors each comprises a field effect transistor.

45. The amplifier of claim 44 wherein the first and second transistors in each amplifying stage comprises a source coupled to its respective common node.

46. The amplifier of claim 45 wherein the first and second transistors in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

47. The amplifier of claim 44 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

48. The amplifier of claim 42 wherein the current switch comprises a transistor.

49 The amplifier of claim 48 wherein the transistor comprises a field effect transistor.

50. The amplifier of claim 49 wherein the transistor comprises a drain coupled to its respective current control input.

51. The amplifier of claim 42 wherein the current switch comprises a current source having a switch control input.

52. The amplifier of claim 51 further comprising a bias circuit coupled to the switch control inputs.

53. The amplifier of claim 52 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

54. The amplifier of claim 53 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

55. The amplifier of claim 54 wherein the summer comprises a cascode current mirror.

56. The amplifier of claim 53 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

57. The amplifier of claim 42 further comprising a matching circuit coupled to the differential output.

58. The amplifier of claim 57 wherein the matching circuit converts a differential current from the differential output to a single-ended current.

59. The amplifier of claim 57 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the amplifying stages is switched in or out of the circuit.

60. The amplifier of claim 57 wherein the differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

61. The amplifier of claim 42 wherein the amplifying stages are coupled together to form a differential input, the amplifier further comprising an input stage coupled to the differential input.

62. The amplifier of claim 22 further comprising a plurality of current switches each coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

63. An amplifier comprising a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level.

64. The amplifier of claim 63 wherein the amplifier comprises CMOS.

65. The amplifier of claim 63 further comprising a plurality of amplifying stages coupled together, each of the amplifying stages having a current control input, and a plurality of current switches to digitally program the power level of the amplifier, the current switches each being coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

66. The amplifier of claim 65 wherein the amplifying stages each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

67. The amplifier of claim 66 wherein the transistors each comprises a field effect transistor.

68. The amplifier of claim 67 wherein the first and second transistors in each amplifying stage comprises a source coupled to its respective common node.

69. The amplifier of claim 68 wherein the first and second transistors in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

70. The amplifier of claim 67 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

71. The amplifier of claim 65 wherein the current switches each comprises a transistor.

72 The amplifier of claim 71 wherein the transistors each comprises a field effect transistor.

73. The amplifier of claim 72 wherein the transistors each comprises a drain coupled to its respective current control input.

74. The amplifier of claim 65 wherein the current switches each comprises a current source having a switch control input.

75. The amplifier of claim 74 further comprising a plurality of bias circuits each coupled to a different one of the switch control inputs.

76. The amplifier of claim 75 wherein the bias circuits each generates a bias current which is substantially independent of temperature, the bias current being applied to its respective switch control input.

77. The amplifier of claim 76 wherein the bias circuits each comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the its respective switch control input.

78. The amplifier of claim 77 wherein the summer comprises a cascode current mirror.

79. The amplifier of claim 76 wherein the current sources each comprises a field effect transistor having a gate comprising the switch control input.

80. An amplifier, comprising:

a plurality of amplifying stages coupled together;

switching means for switching one of the amplifying stages in or out of the amplifier to program power of the amplifier; and

matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power.

81. The amplifier of claim 80 wherein each of said one of the amplifying stage comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

82. The amplifier of claim 81 wherein the transistors each comprises a field effect transistor.

83. The amplifier of claim 82 wherein the first and second transistors each comprises a source coupled to its respective common node.

84. The amplifier of claim 83 wherein the amplifying stages each comprises first and second field effect transistors each having a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

85. The amplifier of claim 82 wherein the amplifying stages each comprises first and second field effect transistors each having a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

86. The amplifier of claim 80 wherein the switching means comprises a transistor.

87 The amplifier of claim 86 wherein the transistor comprises a field effect transistor.

88. The amplifier of claim 87 wherein the transistor comprises a drain coupled to said one of the amplifying stages.

89. The amplifier of claim 80 wherein the switching means comprises a current source having a switch control input.

90. The amplifier of claim 89 further comprising a bias circuit coupled to the switch control input.

91. The amplifier of claim 90 wherein the bias circuit comprises means for generating a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

92. The amplifier of claim 90 wherein the bias circuit comprises means for generating a first bias current exhibiting a positive temperature coefficient, means for generating a second bias current exhibiting a negative temperature coefficient, and means

for summing the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

93. The amplifier of claim 92 wherein the summer comprises a cascode current mirror.

94. The amplifier of claim 80 wherein the matching means comprises means for converting a differential current generated by the amplifier stage to a single-ended current, the single-ended current being coupled to the amplifier output.

95. The amplifier of claim, 80 wherein the amplifying stages comprises a differential output having first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled to the amplifier output.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 15265US01

In the Application of:

Shervin Moloudi et al.

U.S. Serial No.: 09/691,634

Filed: October 18, 2000

For: ADAPTIVE RADIO TRANSCEIVER WITH A POWER AMPLIFIER

Examiner: Marceau Milord

Group Art Unit: 2682

Confirmation No.: 7052

Certificate of Facsimile Transmission

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Michael T. Cruz
Reg. No. 44,636

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is a Brief in support of an Appeal. A Notice of Appeal was received by the United States Patent and Trademark Office on September 2, 2005. A Petition for a One-Month Extension of Time has been enclosed, thereby extending the deadline by which to file an Appeal Brief to December 2, 2005.

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine, California 92618-3616, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment filed with the present application and recorded on Reel 011550, Frame 0086.

RELATED APPEALS AND INTERFERENCES

There are currently no appeals pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-95 are pending in the present application. Pending claims 1-95 have been rejected under 35 U.S.C. § 103(a) and are the subject of this appeal.

STATUS OF THE AMENDMENTS

There are no amendments pending in the present application.

SUMMARY OF THE INVENTION

Some embodiments according to some aspects of the present invention may provide an amplifier that includes, for example, a plurality of differential pairs and a current switch. The plurality of differential pairs may be coupled together through a common differential output. Each differential pair may have a current control input. The current switch may be coupled to the current control input of one of the differential pairs to selectively switch one of the differential pairs in or out of the amplifier.

Some embodiments according to some aspects of the present invention may provide an amplifier that includes, for example, a plurality of amplifying stages and a current switch. The plurality of amplifying stages may each have first and second transistors that may each have first, second and third nodes. The first nodes of the first transistors may be coupled together and the first nodes of the second transistors may be coupled together to form a differential output. The second nodes of the first transistors may be coupled together and the second nodes of the second transistors may be coupled together to form a differential input. The third node of each of the first transistors may be coupled to the third node of its respective second transistor to form a current control input for each of the amplifying stages. The current switch may be coupled to the current control input of one the amplifying stage to switch one of the amplifying stages in or out of the amplifier.

Some embodiments according to some aspects of the present invention may provide an amplifier that may include, for example, a plurality of amplifying stages and a current switch. The plurality of amplifying stages may be coupled together. Each of the amplifying stages may have a current control input. The current switch may be coupled to the current control input of one of the amplifying stages to selectively switch one of the amplifying stages in or out of the circuit.

Some embodiments according to some aspects of the present invention may provide an amplifier that may include, for example, a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level.

Some embodiments according to some aspects of the present invention may provide an amplifier may include, for example, a plurality of amplifying states, switching means and matching means. The plurality of amplifying stages may be coupled together. The switching means may switch one of the amplifying stages in or out of the amplifier to program power of the amplifier. The matching means may match a load coupled to an output of the amplifier. The matching means may be substantially independent of the programmed power.

ISSUES FOR REVIEW

Whether claims 1-18, 20-38, 40-59 and 61-94 are unpatentable under 35 U.S.C. § 103(a) as being obvious over United States Patent No. 6,194,962 B1 to Marcellus R. Chen ("Chen") in view of United States Patent No. 4,901,030 to Stephen P. Webster ("Webster").

Whether claims 19, 39, 60 and 95 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster and further in view of United States Patent No. 6,175,279 B1 to Steven C. Ciccarelli et al. ("Ciccarelli").

GROUPING OF CLAIMS

Claims 1-95 do not stand or fall together.

Group I. Claims 1-21 stand or fall together.

Group II. Claims 22-41 stand or fall together.

Group III. Claims 42-62 stand or fall together.

Group IV. Claims 63-79 stand or fall together.

Group V. Claims 80-95 stand or fall together.

ARGUMENT

I. Group I: Claims 1-21

Claims 1-18, 20 and 21 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 19 stands rejected under 35 U.S.C. § 103(a) as

being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

Appellants respectfully submit that Chen and Webster were improperly combined.

M.P.E.P. § 2145(X)(D)(2) states that "[i]t is improper to combine references where the references teach away from their combination" (citing, e.g., In re Grasselli, 713 F. 2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983)).

In the SUMMARY OF THE INVENTION section of Chen, Chen teaches "[a] system for adaptively trimming the input offset voltage of an op amp ... which overcomes the problems noted [in the BACKGROUND OF THE INVENTION section]". Chen at col. 2, lines 34-36. The pertinent problem in the prior art according to Chen is that rail-to-rail op amps "typically employ complementary differential pairs, instead of the single differential pair found in conventional amplifiers". Chen at col. 1, lines 23-26. "[B]oth differential pairs contribute to the amplifier's offset voltage [V_{os}] .... Unfortunately, V_{os} will change when one or the other of the pairs stop conducting near the supply rail. When this occurs, the trim adjustment made to correct V_{os} when both pairs are active is now incorrect, and V_{os} will increase". Chen at col. 1, lines 56-63. Thus, teachings of Chen are applicable when "[t]he system is used with an op amp having complementary differential pairs in its input stage, which are typically provided to give the op amp a rail-to-rail common-mode input voltage range". Chen at col. 2, lines 40-43 of the SUMMARY OF THE INVENTION section. "The adaptive trimming system is advantageously employed as long as an op amp includes complementary differential pairs in its input stage". Chen at col. 4, lines 59-62.

On the other hand, Webster teaches that "[t]he improved operational amplifier stages are an input, a gain and an output stage". Webster at the Abstract. Webster describes an input stage 601 that includes a *single* pair of transistors Q101, Q102 that are differentially connected. See, e.g., Webster at FIG. 1; and col. 3, lines 37-40. Thus, Webster only teaches a single pair of differential transistors Q101, Q102 in the input

stage 601 and teaches away from "an op amp having complementary differential pairs in its input stage" as taught by Chen. See, e.g., Chen at col. 2, lines 40-43. The system of Chen would not be applicable to the *single* pair of differential transistors Q101, Q102 of the Webster input stage 601 since Chen is solving the problem relating to trimming voltages V_{os} occurring from *two* complementary differential *pairs* as explained above.

Furthermore, the teachings of Chen relate to rail-to-rail op amps which "typically employ complementary differential pairs, instead of the single differential pair found in conventional amplifiers". Chen at col. 1, lines 24-26. Thus, Chen disparages the operational amplifier of Webster as being merely a conventional amplifier.

In addition, Webster does not appear to be a rail-to-rail op amp further teaching away from the combination of Webster and Chen. Chen teaches a system for use with an op amp with "a rail-to-rail common-mode input voltage range" (Chen at col. 2, lines 42-43) in which the op amp "function[s] for input signals that vary up to the amplifier's positive and negative supply voltages" (Chen at col. 1, lines 21-31). On the other hand, Webster does not appear to teach a rail-to-rail op amp. In fact, Webster teaches away from Chen by teaching that "[t]he input stage is operable within a range of differential voltage signals, the range including common mode voltage signals at or beyond the negative supply supply rail." Webster at the Abstract. Webster states "that the common mode input voltage range can include voltages of almost a V_{bc} below the negative supply rail 7". Webster at col. 7, line 68 to col. 8, line 2. Thus, Webster appears to teach away from a rail-to-rail op amp of Chen and appears to teach away from an input stage having two complementary differential transistor pairs as taught by Chen.

Appellants respectfully submit that Chen and Webster were improperly combined since Chen and Webster teach away from each other. Appellants would even go a step further by suggesting that, since the teachings of Chen are used with "an op amp having complementary differential pairs in its input stage, which are typically provided to give the op amp a rail-to-rail common-mode input voltage range", the teachings of Chen would not be applied to the teachings of Webster. Accordingly, Appellants respectfully

submit that there appears to be no suggestion to combine the teachings of Chen and Webster other than impermissible hindsight based on the recited claim elements.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 1 and its rejected dependent claims (i.e., claims 2-21).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 1. Claim 1 recites, for example, "a plurality of differential pairs coupled together though a common differential output".

The Examiner admits that Chen does not teach at least a plurality of differential pairs coupled together through a common differential output. See, e.g., Office Action Made Final of June 29, 2005 at page 2. However, the Examiner offers the teachings of Webster to make up for the teaching deficiencies of Chen. In the Office Action Made Final at page 3, the Examiner is unable to explain where the recited claim elements are in Webster. Instead, the Examiner cites volumes of text: Webster at col. 1, line 41 to col. 2, lines 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52. See Office Action Made Final at page 3.

Webster at col. 1, line 41 to col. 2, line 42 is nothing less than the entire SUMMARY OF THE INVENTION section. The SUMMARY section is broken down to the three main parts of an operational amplifier: an input stage 601, a gain stage 603, and an output stage 605 as illustrated as dashed blocks in FIG. 1 of Webster. Appellants respectfully draw the attention of the Board to FIG. 1 to which the SUMMARY section effectively describes. FIG. 1 of Webster shows the input stage 601, the gain stage 603, the output stage 605 and the bias circuit 607. It is clear that FIG. 1 only shows a single differential pair consisting of transistors Q101, Q102. FIG. 1 does not show "a plurality of differential pairs". Furthermore, the output (i.e., the collector) of transistor Q101 is

connected to the emitter of transistor Q2 and the output (i.e., the collector) of transistor Q102 is connected to the emitter of transistor Q1. Thus, not only does Webster not teach "a plurality of differential pairs", but Webster also does not teach "a plurality of differential pairs coupled together through a common differential output".

Webster at col. 6, line 62 to col. 7, line 66 relates to FIGS. 1 and 4 of Webster. Appellants have already established that FIG. 1 does not teach "a plurality of differential pairs coupled together through a common differential output". Appellants draw the attention of the Board to FIG. 4 of Webster. FIG. 4 shows a schematic of the input stage 601 and part of the bias circuit 607 and part of the gain stage 603. As with FIG. 1, FIG. 4 only shows a single differential pair consisting of the same transistors described above, namely, transistors Q101, Q102. Thus, for the reasons above, not only does FIG. 4 not show "a plurality of differential pairs", FIG. 4 does not show "a plurality of differential pairs coupled together through a common differential output".

Webster at col. 12, lines 15-52 relates to a Darlington pair of transistors. In particular, the Darlington pair of transistors QD, Q9 is illustrated in FIGS. 11 and 12. Appellants respectfully submit that a Darlington pair is not a differential pair of transistors. Appellants respectfully draw the attention to transistors QD, Q9 in FIG. 11 which show that configuration is not a differential pair configuration. FIG. 12 shows another embodiment of transistor QD. Transistor QD, in FIG. 12, comprises current mirror transistors Q104A, Q104B, transistor Q8, resistor R4 and transistor Q105. Appellants respectfully submit that FIGS. 11 and 12 of Webster do not show any differential pairs and thus do not show "a plurality of differential pairs". Furthermore, FIGS. 11 and 12 of Webster do not show "a plurality of differential pairs coupled together through a common differential output".

Having analyzed all the text in Webster cited by the Examiner in support of the obviousness rejection, it appears that Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52 and any and all the figures associated with the cited text do not teach "a plurality of differential pairs" and, in particular, the

cited text and accompanying figures of Webster do not teach "a plurality of differential pairs coupled together through a common differential output".

In the Response to Arguments section of the Office Action Made Final, the Examiner declares that "Applicant's arguments filed on 3-4-2005 have been fully considered by they are not persuasive". The Examiner further declares that FIG. 1 and 2 show "a balanced type differential type amplifier circuit that comprises a mutual conductance differential amplifier circuit having two differential output terminals, a constant-current circuit and a detector (col. 1, lines 43-54; col. 1, line 64 - col. 2, line 10). It is considered that this balance type differential amplifier can be constituted a plurality of differential pairs".

Appellants respectfully draw the attention of the Board to the arguments and rebuttal evidence as set forth above in support of Appellants' conclusion that Webster does not teach "a plurality of differential pairs coupled together through a common differential output". Appellants respectfully draw the attention of the Board to FIG. 1 and, in particular, to the input stage 601 which has a single pair of differential transistors Q101, Q102 and not a plurality of differential transistors. Multiple differential pairs are not taught by the input stage 601 of Webster. Furthermore, no common differential output is shown in FIG. 1. The Examiner alleged "two differential output terminals" in the Office Action Made Final at page 20; however, Webster shows no such output terminals. At the most, Webster shows a single-ended amplifier output at, for example, output 15 of transistor Q9.

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 1. Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 1 and its rejected dependent claims (i.e., claims 2-21).

II. Group II: Claims 22-41

Claims 22-38, 40 and 41 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 39 stands rejected under 35 U.S.C. § 103(a) as being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 22-41.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 22 and its rejected dependent claims (i.e., claims 23-41).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 22. Claim 22 recites, for example, "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output".

The Examiner admits that Chen does not teach at least first nodes of first transistors being coupled together and first nodes of second transistors being coupled together to form a differential output. See, e.g., Office Action Made Final of June 29, 2005 at page 7. However, the Examiner offers the teachings of Webster to make up for the teaching deficiencies of Chen. In the Office Action Made Final at page 7, the Examiner is unable to explain where the recited claim elements are in Webster. Instead, the Examiner cites volumes of text: Webster at col. 1, line 41 to col. 2, lines 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52. See Office Action Made Final at page 7.

Webster at col. 1, line 41 to col. 2, line 42 is nothing less than the entire SUMMARY OF THE INVENTION section. The SUMMARY section is broken down to the three main parts of an operational amplifier: an input stage 601, a gain stage 603, and an output stage 605 as illustrated as dashed blocks in FIG. 1 of Webster. Appellants respectfully draw the attention of the Board to FIG. 1 to which the SUMMARY section effectively describes. FIG. 1 of Webster shows the input stage 601, the gain stage 603, the output stage 605 and the bias circuit 607. It is clear that FIG. 1 only shows a single differential pair consisting of transistors Q101, Q102. FIG. 1 does not show "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set froth in claim 22. The output (i.e., the collector) of transistor Q101 is connected to the emitter of transistor Q2 and the output (i.e., the collector) of transistor Q102 is connected to the emitter of transistor Q1. Thus, Webster not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

Webster at col. 6, line 62 to col. 7, line 66 relates to FIGS. 1 and 4 of Webster. Appellants have already established that FIG. 1 does not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22. Appellants respectfully draw the attention of the Board to FIG. 4 of Webster. FIG. 4 shows a schematic of the input stage 601 and part of the bias circuit 607 and part of the gain stage 603. FIG. 4 does not show "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

Webster at col. 12, lines 15-52 relates to a Darlington pair of transistors. In particular, the Darlington pair of transistors QD, Q9 is illustrated in FIGS. 11 and 12. FIG. 12 shows another embodiment of transistor QD. Transistor QD, in FIG. 12, comprises current mirror transistors Q104A, Q104B, transistor Q8, resistor R4 and transistor Q105. Appellants respectfully submit that FIGS. 11 and 12 of Webster do not show "the first nodes of the first transistors being coupled together and the first nodes of

the second transistors being coupled together to form a differential output" as set forth in claim 22.

Having analyzed all the text in Webster cited by the Examiner in support of the obviousness rejection, it appears that Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52 and any and all the figures associated with the cited text do not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

In the Response to Arguments section of the Office Action Made Final, the Examiner declares that "Applicant's arguments filed on 3-4-2005 have been fully considered by they are not persuasive". The Examiner further declares that FIG. 1 and 2 show "a balanced type differential type amplifier circuit that comprises a mutual conductance differential amplifier circuit having two differential output terminals, a constant-current circuit and a detector (col. 1, lines 43-54; col. 1, line 64 - col. 2, line 10). It is considered that this balance type differential amplifier can be constituted a plurality of differential pairs".

Appellants respectfully draw the attention of the Board to the arguments and rebuttal evidence as set forth above in support of Appellants' conclusion that Webster does not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 22. Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 22 and its rejected dependent claims (i.e., claims 23-41).

III. Group III: Claims 42-62

Claims 42-59, 61 and 62 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 60 stands rejected under 35 U.S.C. § 103(a) as being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 42-62.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 42 and its rejected dependent claims (i.e., claims 43-62).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 42.

The Examiner admits that Chen does not teach at least "a current switch coupled to the current control input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit". To make up for the teaching deficiencies of Chen, the Examiner further alleges that Webster teaches at least these elements. To support this assertion, the Examiner cites the same text as before with respect to the rejection of claims 1 and 22, namely, Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52. Appellants respectfully submit that the cited text and corresponding figures in Webster do not teach *selectively* switching an amplifying stage of a plurality of amplifying stages in or out of a circuit. Furthermore, Webster does not teach "a current switch coupled to the current control

input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit" as set forth in claim 42.

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 42. Accordingly, Appellants have successfully traversed the obviousness rejection with respect to claim 42 and its dependent claims (i.e., claims 43-62).

IV. Group IV: Claims 63-79

Claims 63-79 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 63-79.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 63 and its rejected dependent claims (i.e., claims 63-79).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 63. Claim 63 recites, for example, "a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level". The Examiner maintains that these elements are illustrated in Chen at FIGS. 3 and 4 and described in Chen at col. 2, lines 41-61; col. 3, lines 38-57; and col. 5, lines 3-32. Appellants have carefully reviewed the cited portions

of Chen and cannot find support for a digitally programmable power level and a matching circuit and, in particular, a matching circuit that is substantially independent of the programmed power level. For at least the above reasons, Chen in view of Webster does not render obvious the subject matter recited in claim 63 and its rejected dependent claims (i.e., claims 64-79).

Since Webster does not make up for the teaching deficiencies of Chen and the Examiner makes no such allegation or *prima facie* case in the Office Action Made Final, Chen in view of Webster does not teach each and every element as set forth in claim 63.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 63 and its dependent claims (i.e., claims 64-79).

V. Group V: Claims 80-95

Claims 80-94 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 95 stands rejected under 35 U.S.C. § 103(a) as being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 80-95.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 80 and its rejected dependent claims (i.e., claims 81-95).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For

example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 80. Claim 80 recites, for example, "matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power".

Neither Chen nor Webster, individually or combined, teaches each and every element as set forth in claim 80. For example, claim 80 recites "matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power". Since there is no mention of the load coupled to the output stage 34 of the op amp, Chen does not teach any type of matching with respect to such a load. Instead, Chen is merely concerned with trimming an op amp offset voltage. On the other hand, Webster does not teach at least matching means for matching a load coupled to an output of the amplifier. Webster is silent as to matching a load. Since Webster does not make up for the teaching deficiencies of Chen and the Examiner makes no such allegation or *prima facie* case in the Office Action Made Final, Chen in view of Webster does not teach each and every element as set forth in claim 63. For at least the above reasons, neither Chen nor Webster, individually or combined, renders obvious the subject matter recited in claim 80 and its rejected dependent claims (i.e., claims 81-95).

Accordingly, it is respectfully requested that the Board reverse the obviousness rejection with respect to claim 80 and its rejected dependent claims (i.e., claims 81-95).

VI. Conclusion

For the foregoing reasons, claims 1-95 are distinguishable over the prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: December 2, 2005

Respectfully submitted,

Michael T. Cruz
Registration No. 44,636
Attorney for Appellants

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8084
Facsimile: (312) 775-8100

APPENDIX

The following claims are involved in this appeal:

1. An amplifier, comprising:

a plurality of differential pairs coupled together through a common differential output, each differential pair having a current control input; and

a current switch coupled to the current control input of one of the differential pairs to selectively switch said one of the differential pairs in or out of the amplifier.

2. The amplifier of claim 1 wherein the differential pairs each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

3. The amplifier of claim 2 wherein the transistors each comprises a field effect transistor

4. The amplifier of claim 3 wherein the first and second transistors in each differential pair each comprises a source coupled to its respective common node.

5. The amplifier of claim 4 wherein the first and second transistors in each of the differential pairs each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

6. The amplifier of claim 3 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form the differential output.

7. The amplifier of claim 1 wherein the current switch comprises a transistor.

8 The amplifier of claim 7 wherein the transistor comprises a field effect transistor.

9. The amplifier of claim 8 wherein the transistor comprises a drain coupled to its respective current control input.

10. The amplifier of claim 1 wherein the current switch comprises a current source having a switch control input.

11. The amplifier of claim 10 further comprising a bias circuit coupled to the switch control input.

12. The amplifier of claim 11 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

13. The amplifier of claim 12 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

14. The amplifier of claim 13 wherein the summer comprises a cascode current mirror.

15. The amplifier of claim 12 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

16. The amplifier of claim 1 further comprising a matching circuit coupled to the common differential output.

17. The amplifier of claim 16 wherein the matching circuit converts a differential current from the common differential output to a single-ended current.

18. The amplifier of claim 16 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the differential pairs is switched in or out of the amplifier.

19. The amplifier of claim 16 wherein the common differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

20. The amplifier of claim 1 wherein the differential pairs are further coupled together through a common differential input, the amplifier further comprising an input stage coupled to the common differential input.

21. The amplifier of claim 1 further comprising a plurality of current switches each coupled to the current control input for a different one of the differential pairs to selectively switch its respective differential pair in or out of the amplifier.

22. An amplifier, comprising:

a plurality of amplifying stages each having first and second transistors, the first and second transistors each having first, second and third nodes, the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output, the second nodes of the first transistors being coupled together and the second nodes of the second transistors being coupled together to form a differential input, and the third node of each of the first transistors being coupled to the third node of its respective second transistor to form a current control input for each of the amplifying stages; and

a current switch coupled to the current control input of one the amplifying stage to switch said one of the amplifying stages in or out of the amplifier.

23. The amplifier of claim 22 wherein the transistors each comprises a field effect transistor.

24. The amplifier of claim 23 wherein the third nodes each comprises a source.

25. The amplifier of claim 24 wherein the second nodes each comprises a gate.

26. The amplifier of claim 23 wherein the first nodes each comprises a drain.

27. The amplifier of claim 22 wherein the current switch comprises a transistor.

28. The amplifier of claim 27 wherein the transistor comprises a field effect transistor.

29. The amplifier of claim 28 wherein the transistor comprises a drain coupled to its respective current control input.

30. The amplifier of claim 22 wherein the current switch comprises a current source having a switch control input.

31. The amplifier of claim 30 further comprising a bias circuit coupled to the switch control input.

32. The amplifier of claim 31 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied the switch control input.

33. The amplifier of claim 32 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

34. The amplifier of claim 33 wherein the summer comprises a cascode current mirror.

35. The amplifier of claim 34 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

36. The amplifier of claim 22 further comprising a matching circuit coupled to the differential output.

37. The amplifier of claim 36 wherein the matching circuit converts a differential current from the differential output to a single-ended current.

38. The amplifier of claim 36 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the amplifying stages is switched in or out of the circuit.

39. The amplifier of claim 36 wherein the common differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

40. The amplifier of claim 22 further comprising an input stage coupled to the differential input.

41. The amplifier of claim 22 further comprising a plurality of current switches each coupled the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

42. An amplifier, comprising:

a plurality of amplifying stages coupled together, each of the amplifying stages having a current control input; and

a current switch coupled to the current control input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit.

43. The amplifier of claim 42 wherein the amplifying stages each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

44. The amplifier of claim 43 wherein the transistors each comprises a field effect transistor.

45. The amplifier of claim 44 wherein the first and second transistors in each amplifying stage comprises a source coupled to its respective common node.

46. The amplifier of claim 45 wherein the first and second transistors in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

47. The amplifier of claim 44 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

48. The amplifier of claim 42 wherein the current switch comprises a transistor.

49 The amplifier of claim 48 wherein the transistor comprises a field effect transistor.

50. The amplifier of claim 49 wherein the transistor comprises a drain coupled to its respective current control input.

51. The amplifier of claim 42 wherein the current switch comprises a current source having a switch control input.

52. The amplifier of claim 51 further comprising a bias circuit coupled to the switch control inputs.

53. The amplifier of claim 52 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

54. The amplifier of claim 53 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

55. The amplifier of claim 54 wherein the summer comprises a cascode current mirror.

56. The amplifier of claim 53 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

57. The amplifier of claim 42 further comprising a matching circuit coupled to the differential output.

58. The amplifier of claim 57 wherein the matching circuit converts a differential current from the differential output to a single-ended current.

59. The amplifier of claim 57 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the amplifying stages is switched in or out of the circuit.

60. The amplifier of claim 57 wherein the differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

61. The amplifier of claim 42 wherein the amplifying stages are coupled together to form a differential input, the amplifier further comprising an input stage coupled to the differential input.

62. The amplifier of claim 22 further comprising a plurality of current switches each coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

63. An amplifier comprising a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level.

64. The amplifier of claim 63 wherein the amplifier comprises CMOS.

65. The amplifier of claim 63 further comprising a plurality of amplifying stages coupled together, each of the amplifying stages having a current control input, and a plurality of current switches to digitally program the power level of the amplifier, the current switches each being coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

66. The amplifier of claim 65 wherein the amplifying stages each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

67. The amplifier of claim 66 wherein the transistors each comprises a field effect transistor.

68. The amplifier of claim 67 wherein the first and second transistors in each amplifying stage comprises a source coupled to its respective common node.

69. The amplifier of claim 68 wherein the first and second transistors in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

70. The amplifier of claim 67 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

71. The amplifier of claim 65 wherein the current switches each comprises a transistor.

72 The amplifier of claim 71 wherein the transistors each comprises a field effect transistor.

73. The amplifier of claim 72 wherein the transistors each comprises a drain coupled to its respective current control input.

74. The amplifier of claim 65 wherein the current switches each comprises a current source having a switch control input.

75. The amplifier of claim 74 further comprising a plurality of bias circuits each coupled to a different one of the switch control inputs.

76. The amplifier of claim 75 wherein the bias circuits each generates a bias current which is substantially independent of temperature, the bias current being applied to its respective switch control input.

77. The amplifier of claim 76 wherein the bias circuits each comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the its respective switch control input.

78. The amplifier of claim 77 wherein the summer comprises a cascode current mirror.

79. The amplifier of claim 76 wherein the current sources each comprises a field effect transistor having a gate comprising the switch control input.

80. An amplifier, comprising:

a plurality of amplifying stages coupled together;

switching means for switching one of the amplifying stages in or out of the amplifier to program power of the amplifier; and

matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power.

81. The amplifier of claim 80 wherein each of said one of the amplifying stage comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

82. The amplifier of claim 81 wherein the transistors each comprises a field effect transistor.

83. The amplifier of claim 82 wherein the first and second transistors each comprises a source coupled to its respective common node.

84. The amplifier of claim 83 wherein the amplifying stages each comprises first and second field effect transistors each having a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

85. The amplifier of claim 82 wherein the amplifying stages each comprises first and second field effect transistors each having a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

86. The amplifier of claim 80 wherein the switching means comprises a transistor.

87 The amplifier of claim 86 wherein the transistor comprises a field effect transistor.

88. The amplifier of claim 87 wherein the transistor comprises a drain coupled to said one of the amplifying stages.

89. The amplifier of claim 80 wherein the switching means comprises a current source having a switch control input.

90. The amplifier of claim 89 further comprising a bias circuit coupled to the switch control input.

91. The amplifier of claim 90 wherein the bias circuit comprises means for generating a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

92. The amplifier of claim 90 wherein the bias circuit comprises means for generating a first bias current exhibiting a positive temperature coefficient, means for generating a second bias current exhibiting a negative temperature coefficient, and means

for summing the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

93. The amplifier of claim 92 wherein the summer comprises a cascode current mirror.

94. The amplifier of claim 80 wherein the matching means comprises means for converting a differential current generated by the amplifier stage to a single-ended current, the single-ended current being coupled to the amplifier output.

95. The amplifier of claim, 80 wherein the amplifying stages comprises a differential output having first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled to the amplifier output.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 15265US01

In the Application of:

Shervin Moloudi et al.

U.S. Serial No.: 09/691,634

Filed: October 18, 2000

For: ADAPTIVE RADIO TRANSCEIVER WITH A POWER AMPLIFIER

Examiner: Marceau Milord

Group Art Unit: 2682

Confirmation No.: 7052

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Michael T. Cruz
Reg. No. 44,636

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is a Brief in support of an Appeal. A Notice of Appeal was received by the United States Patent and Trademark Office on September 2, 2005. A Petition for a One-Month Extension of Time has been enclosed, thereby extending the deadline by which to file an Appeal Brief to December 2, 2005.

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine, California 92618-3616, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment filed with the present application and recorded on Reel 011550, Frame 0086.

RELATED APPEALS AND INTERFERENCES

There are currently no appeals pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-95 are pending in the present application. Pending claims 1-95 have been rejected under 35 U.S.C. § 103(a) and are the subject of this appeal.

~~STATUS~~ OF THE AMENDMENTS

There are no amendments pending in the present application.

SUMMARY OF THE INVENTION

Some embodiments according to some aspects of the present invention may provide an amplifier that includes, for example, a plurality of differential pairs and a current switch. The plurality of differential pairs may be coupled together through a common differential output. Each differential pair may have a current control input. The current switch may be coupled to the current control input of one of the differential pairs to selectively switch one of the differential pairs in or out of the amplifier.

Some embodiments according to some aspects of the present invention may provide an amplifier that includes, for example, a plurality of amplifying stages and a current switch. The plurality of amplifying stages may each have first and second transistors that may each have first, second and third nodes. The first nodes of the first transistors may be coupled together and the first nodes of the second transistors may be coupled together to form a differential output. The second nodes of the first transistors may be coupled together and the second nodes of the second transistors may be coupled together to form a differential input. The third node of each of the first transistors may be coupled to the third node of its respective second transistor to form a current control input for each of the amplifying stages. The current switch may be coupled to the current control input of one the amplifying stage to switch one of the amplifying stages in or out of the amplifier.

Some embodiments according to some aspects of the present invention may provide an amplifier that may include, for example, a plurality of amplifying stages and a current switch. The plurality of amplifying stages may be coupled together. Each of the amplifying stages may have a current control input. The current switch may be coupled to the current control input of one of the amplifying stages to selectively switch one of the amplifying stages in or out of the circuit.

Some embodiments according to some aspects of the present invention may provide an amplifier that may include, for example, a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level.

Some embodiments according to some aspects of the present invention may provide an amplifier may include, for example, a plurality of amplifying states, switching means and matching means. The plurality of amplifying stages may be coupled together. The switching means may switch one of the amplifying stages in or out of the amplifier to program power of the amplifier. The matching means may match a load coupled to an output of the amplifier. The matching means may be substantially independent of the programmed power.

ISSUES FOR REVIEW

Whether claims 1-18, 20-38, 40-59 and 61-94 are unpatentable under 35 U.S.C. § 103(a) as being obvious over United States Patent No. 6,194,962 B1 to Marcellus R. Chen ("Chen") in view of United States Patent No. 4,901,030 to Stephen P. Webster ("Webster").

Whether claims 19, 39, 60 and 95 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster and further in view of United States Patent No. 6,175,279 B1 to Steven C. Ciccarelli et al. ("Ciccarelli").

GROUPING OF CLAIMS

Claims 1-95 do not stand or fall together.

Group I. Claims 1-21 stand or fall together.

Group II. Claims 22-41 stand or fall together.

Group III. Claims 42-62 stand or fall together.

Group IV. Claims 63-79 stand or fall together.

Group V. Claims 80-95 stand or fall together.

ARGUMENT

I. Group I: Claims 1-21

Claims 1-18, 20 and 21 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 19 stands rejected under 35 U.S.C. § 103(a) as

being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

Appellants respectfully submit that Chen and Webster were improperly combined.

M.P.E.P. § 2145(X)(D)(2) states that "[i]t is improper to combine references where the references teach away from their combination" (citing, e.g., In re Grasselli, 713 F. 2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983)).

In the SUMMARY OF THE INVENTION section of Chen, Chen teaches "[a] system for adaptively trimming the input offset voltage of an op amp ... which overcomes the problems noted [in the BACKGROUND OF THE INVENTION section]". Chen at col. 2, lines 34-36. The pertinent problem in the prior art according to Chen is that rail-to-rail op amps "typically employ complementary differential pairs, instead of the single differential pair found in conventional amplifiers". Chen at col. 1, lines 23-26. "[B]oth differential pairs contribute to the amplifier's offset voltage [V_{os}] .... Unfortunately, V_{os} will change when one or the other of the pairs stop conducting near the supply rail. When this occurs, the trim adjustment made to correct V_{os} when both pairs are active is now incorrect, and V_{os} will increase". Chen at col. 1, lines 56-63. Thus, teachings of Chen are applicable when "[t]he system is used with an op amp having complementary differential pairs in its input stage, which are typically provided to give the op amp a rail-to-rail common-mode input voltage range". Chen at col. 2, lines 40-43 of the SUMMARY OF THE INVENTION section. "The adaptive trimming system is advantageously employed as long as an op amp includes complementary differential pairs in its input stage". Chen at col. 4, lines 59-62.

On the other hand, Webster teaches that "[t]he improved operational amplifier stages are an input, a gain and an output stage". Webster at the Abstract. Webster describes an input stage 601 that includes a *single* pair of transistors Q101, Q102 that are differentially connected. See, e.g., Webster at FIG. 1; and col. 3, lines 37-40. Thus, Webster only teaches a single pair of differential transistors Q101, Q102 in the input

stage 601 and teaches away from "an op amp having complementary differential pairs in its input stage" as taught by Chen. See, e.g., Chen at col. 2, lines 40-43. The system of Chen would not be applicable to the *single* pair of differential transistors Q101, Q102 of the Webster input stage 601 since Chen is solving the problem relating to trimming voltages V_{os} occurring from *two* complementary differential *pairs* as explained above.

Furthermore, the teachings of Chen relate to rail-to-rail op amps which "typically employ complementary differential pairs, instead of the single differential pair found in conventional amplifiers". Chen at col. 1, lines 24-26. Thus, Chen disparages the operational amplifier of Webster as being merely a conventional amplifier.

In addition, Webster does not appear to be a rail-to-rail op amp further teaching away from the combination of Webster and Chen. Chen teaches a system for use with an op amp with "a rail-to-rail common-mode input voltage range" (Chen at col. 2, lines 42-43) in which the op amp "function[s] for input signals that vary up to the amplifier's positive and negative supply voltages" (Chen at col. 1, lines 21-31). On the other hand, Webster does not appear to teach a rail-to-rail op amp. In fact, Webster teaches away from Chen by teaching that "[t]he input stage is operable within a range of differential voltage signals, the range including common mode voltage signals at or beyond the negative supply supply rail." Webster at the Abstract. Webster states "that the common mode input voltage range can include voltages of almost a V_{be} below the negative supply rail 7". Webster at col. 7, line 68 to col. 8, line 2. Thus, Webster appears to teach away from a rail-to-rail op amp of Chen and appears to teach away from an input stage having two complementary differential transistor pairs as taught by Chen.

Appellants respectfully submit that Chen and Webster were improperly combined since Chen and Webster teach away from each other. Appellants would even go a step further by suggesting that, since the teachings of Chen are used with "an op amp having complementary differential pairs in its input stage, which are typically provided to give the op amp a rail-to-rail common-mode input voltage range", the teachings of Chen would not be applied to the teachings of Webster. Accordingly, Appellants respectfully

submit that there appears to be no suggestion to combine the teachings of Chen and Webster other than impermissible hindsight based on the recited claim elements.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 1 and its rejected dependent claims (i.e., claims 2-21).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 1. Claim 1 recites, for example, "a plurality of differential pairs coupled together though a common differential output".

The Examiner admits that Chen does not teach at least a plurality of differential pairs coupled together through a common differential output. See, e.g., Office Action Made Final of June 29, 2005 at page 2. However, the Examiner offers the teachings of Webster to make up for the teaching deficiencies of Chen. In the Office Action Made Final at page 3, the Examiner is unable to explain where the recited claim elements are in Webster. Instead, the Examiner cites volumes of text: Webster at col. 1, line 41 to col. 2, lines 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52. See Office Action Made Final at page 3.

Webster at col. 1, line 41 to col. 2, line 42 is nothing less than the entire SUMMARY OF THE INVENTION section. The SUMMARY section is broken down to the three main parts of an operational amplifier: an input stage 601, a gain stage 603, and an output stage 605 as illustrated as dashed blocks in FIG. 1 of Webster. Appellants respectfully draw the attention of the Board to FIG. 1 to which the SUMMARY section effectively describes. FIG. 1 of Webster shows the input stage 601, the gain stage 603, the output stage 605 and the bias circuit 607. It is clear that FIG. 1 only shows a single differential pair consisting of transistors Q101, Q102. FIG. 1 does not show "a plurality of differential pairs". Furthermore, the output (i.e., the collector) of transistor Q101 is

connected to the emitter of transistor Q2 and the output (i.e., the collector) of transistor Q102 is connected to the emitter of transistor Q1. Thus, not only does Webster not teach "a plurality of differential pairs", but Webster also does not teach "a plurality of differential pairs coupled together through a common differential output".

Webster at col. 6, line 62 to col. 7, line 66 relates to FIGS. 1 and 4 of Webster. Appellants have already established that FIG. 1 does not teach "a plurality of differential pairs coupled together through a common differential output". Appellants draw the attention of the Board to FIG. 4 of Webster. FIG. 4 shows a schematic of the input stage 601 and part of the bias circuit 607 and part of the gain stage 603. As with FIG. 1, FIG. 4 only shows a single differential pair consisting of the same transistors described above, namely, transistors Q101, Q102. Thus, for the reasons above, not only does FIG. 4 not show "a plurality of differential pairs", FIG. 4 does not show "a plurality of differential pairs coupled together through a common differential output".

Webster at col. 12, lines 15-52 relates to a Darlington pair of transistors. In particular, the Darlington pair of transistors QD, Q9 is illustrated in FIGS. 11 and 12. Appellants respectfully submit that a Darlington pair is not a differential pair of transistors. Appellants respectfully draw the attention to transistors QD, Q9 in FIG. 11 which show that configuration is not a differential pair configuration. FIG. 12 shows another embodiment of transistor QD. Transistor QD, in FIG. 12, comprises current mirror transistors Q104A, Q104B, transistor Q8, resistor R4 and transistor Q105. Appellants respectfully submit that FIGS. 11 and 12 of Webster do not show any differential pairs and thus do not show "a plurality of differential pairs". Furthermore, FIGS. 11 and 12 of Webster do not show "a plurality of differential pairs coupled together through a common differential output".

Having analyzed all the text in Webster cited by the Examiner in support of the obviousness rejection, it appears that Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52 and any and all the figures associated with the cited text do not teach "a plurality of differential pairs" and, in particular, the

cited text and accompanying figures of Webster do not teach "a plurality of differential pairs coupled together through a common differential output".

In the Response to Arguments section of the Office Action Made Final, the Examiner declares that "Applicant's arguments filed on 3-4-2005 have been fully considered by they are not persuasive". The Examiner further declares that FIG. 1 and 2 show "a balanced type differential type amplifier circuit that comprises a mutual conductance differential amplifier circuit having two differential output terminals, a constant-current circuit and a detector (col. 1, lines 43-54; col. 1, line 64 - col. 2, line 10). It is considered that this balance type differential amplifier can be constituted a plurality of differential pairs".

Appellants respectfully draw the attention of the Board to the arguments and rebuttal evidence as set forth above in support of Appellants' conclusion that Webster does not teach "a plurality of differential pairs coupled together through a common differential output". Appellants respectfully draw the attention of the Board to FIG. 1 and, in particular, to the input stage 601 which has a single pair of differential transistors Q101, Q102 and not a plurality of differential transistors. Multiple differential pairs are not taught by the input stage 601 of Webster. Furthermore, no common differential output is shown in FIG. 1. The Examiner alleged "two differential output terminals" in the Office Action Made Final at page 20; however, Webster shows no such output terminals. At the most, Webster shows a single-ended amplifier output at, for example, output 15 of transistor Q9.

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 1. Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 1 and its rejected dependent claims (i.e., claims 2-21).

II. Group II: Claims 22-41

Claims 22-38, 40 and 41 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 39 stands rejected under 35 U.S.C. § 103(a) as being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 22-41.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 22 and its rejected dependent claims (i.e., claims 23-41).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 22. Claim 22 recites, for example, "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output".

The Examiner admits that Chen does not teach at least first nodes of first transistors being coupled together and first nodes of second transistors being coupled together to form a differential output. See, e.g., Office Action Made Final of June 29, 2005 at page 7. However, the Examiner offers the teachings of Webster to make up for the teaching deficiencies of Chen. In the Office Action Made Final at page 7, the Examiner is unable to explain where the recited claim elements are in Webster. Instead, the Examiner cites volumes of text: Webster at col. 1, line 41 to col. 2, lines 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52. See Office Action Made Final at page 7.

Webster at col. 1, line 41 to col. 2, line 42 is nothing less than the entire SUMMARY OF THE INVENTION section. The SUMMARY section is broken down to the three main parts of an operational amplifier: an input stage 601, a gain stage 603, and an output stage 605 as illustrated as dashed blocks in FIG. 1 of Webster. Appellants respectfully draw the attention of the Board to FIG. 1 to which the SUMMARY section effectively describes. FIG. 1 of Webster shows the input stage 601, the gain stage 603, the output stage 605 and the bias circuit 607. It is clear that FIG. 1 only shows a single differential pair consisting of transistors Q101, Q102. FIG. 1 does not show "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set froth in claim 22. The output (i.e., the collector) of transistor Q101 is connected to the emitter of transistor Q2 and the output (i.e., the collector) of transistor Q102 is connected to the emitter of transistor Q1. Thus, Webster not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

Webster at col. 6, line 62 to col. 7, line 66 relates to FIGS. 1 and 4 of Webster. Appellants have already established that FIG. 1 does not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22. Appellants respectfully draw the attention of the Board to FIG. 4 of Webster. FIG. 4 shows a schematic of the input stage 601 and part of the bias circuit 607 and part of the gain stage 603. FIG. 4 does not show "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

Webster at col. 12, lines 15-52 relates to a Darlington pair of transistors. In particular, the Darlington pair of transistors QD, Q9 is illustrated in FIGS. 11 and 12. FIG. 12 shows another embodiment of transistor QD. Transistor QD, in FIG. 12, comprises current mirror transistors Q104A, Q104B, transistor Q8, resistor R4 and transistor Q105. Appellants respectfully submit that FIGS. 11 and 12 of Webster do not show "the first nodes of the first transistors being coupled together and the first nodes of

the second transistors being coupled together to form a differential output" as set forth in claim 22.

Having analyzed all the text in Webster cited by the Examiner in support of the obviousness rejection, it appears that Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52 and any and all the figures associated with the cited text do not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

In the Response to Arguments section of the Office Action Made Final, the Examiner declares that "Applicant's arguments filed on 3-4-2005 have been fully considered by they are not persuasive". The Examiner further declares that FIG. 1 and 2 show "a balanced type differential type amplifier circuit that comprises a mutual conductance differential amplifier circuit having two differential output terminals, a constant-current circuit and a detector (col. 1, lines 43-54; col. 1, line 64 - col. 2, line 10). It is considered that this balance type differential amplifier can be constituted a plurality of differential pairs".

Appellants respectfully draw the attention of the Board to the arguments and rebuttal evidence as set forth above in support of Appellants' conclusion that Webster does not teach "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22.

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 22. Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 22 and its rejected dependent claims (i.e., claims 23-41).

III. Group III: Claims 42-62

Claims 42-59, 61 and 62 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 60 stands rejected under 35 U.S.C. § 103(a) as being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 42-62.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 42 and its rejected dependent claims (i.e., claims 43-62).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 42.

The Examiner admits that Chen does not teach at least "a current switch coupled to the current control input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit". To make up for the teaching deficiencies of Chen, the Examiner further alleges that Webster teaches at least these elements. To support this assertion, the Examiner cites the same text as before with respect to the rejection of claims 1 and 22, namely, Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52. Appellants respectfully submit that the cited text and corresponding figures in Webster do not teach *selectively* switching an amplifying stage of a plurality of amplifying stages in or out of a circuit. Furthermore, Webster does not teach "a current switch coupled to the current control

input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit" as set forth in claim 42.

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 42. Accordingly, Appellants have successfully traversed the obviousness rejection with respect to claim 42 and its dependent claims (i.e., claims 43-62).

IV. Group IV: Claims 63-79

Claims 63-79 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 63-79.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 63 and its rejected dependent claims (i.e., claims 63-79).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 63. Claim 63 recites, for example, "a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level". The Examiner maintains that these elements are illustrated in Chen at FIGS. 3 and 4 and described in Chen at col. 2, lines 41-61; col. 3, lines 38-57; and col. 5, lines 3-32. Appellants have carefully reviewed the cited portions

of Chen and cannot find support for a digitally programmable power level and a matching circuit and, in particular, a matching circuit that is substantially independent of the programmed power level. For at least the above reasons, Chen in view of Webster does not render obvious the subject matter recited in claim 63 and its rejected dependent claims (i.e., claims 64-79).

Since Webster does not make up for the teaching deficiencies of Chen and the Examiner makes no such allegation or *prima facie* case in the Office Action Made Final, Chen in view of Webster does not teach each and every element as set forth in claim 63.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 63 and its dependent claims (i.e., claims 64-79).

V. Group V: Claims 80-95

Claims 80-94 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster. Claim 95 stands rejected under 35 U.S.C. § 103(a) as being over Chen in view of Webster and further in view of Ciccarelli. Appellants respectfully request that the Board reverse the rejection for the reasons set forth below.

A. Improper Combination of Chen and Webster

The arguments made and the rebuttal evidence presented in section I.A. above with respect to claims 1-21 are made and presented here with respect to claims 80-95.

Accordingly, it is respectfully requested that the Board reverse the rejection with respect to claim 80 and its rejected dependent claims (i.e., claims 81-95).

B. Each and Every Element Not Taught

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Appellants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For

example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 80. Claim 80 recites, for example, "matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power".

Neither Chen nor Webster, individually or combined, teaches each and every element as set forth in claim 80. For example, claim 80 recites "matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power". Since there is no mention of the load coupled to the output stage 34 of the op amp, Chen does not teach any type of matching with respect to such a load. Instead, Chen is merely concerned with trimming an op amp offset voltage. On the other hand, Webster does not teach at least matching means for matching a load coupled to an output of the amplifier. Webster is silent as to matching a load. Since Webster does not make up for the teaching deficiencies of Chen and the Examiner makes no such allegation or *prima facie* case in the Office Action Made Final, Chen in view of Webster does not teach each and every element as set forth in claim 63. For at least the above reasons, neither Chen nor Webster, individually or combined, renders obvious the subject matter recited in claim 80 and its rejected dependent claims (i.e., claims 81-95).

Accordingly, it is respectfully requested that the Board reverse the obviousness rejection with respect to claim 80 and its rejected dependent claims (i.e., claims 81-95).

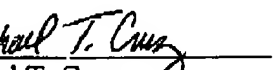
VI. Conclusion

For the foregoing reasons, claims 1-95 are distinguishable over the prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: December 2, 2005

Respectfully submitted,



Michael T. Cruz
Registration No. 44,636
Attorney for Appellants

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8084
Facsimile: (312) 775-8100

APPENDIX

The following claims are involved in this appeal:

1. An amplifier, comprising:

a plurality of differential pairs coupled together through a common differential output, each differential pair having a current control input; and

a current switch coupled to the current control input of one of the differential pairs to selectively switch said one of the differential pairs in or out of the amplifier.

2. The amplifier of claim 1 wherein the differential pairs each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

3. The amplifier of claim 2 wherein the transistors each comprises a field effect transistor

4. The amplifier of claim 3 wherein the first and second transistors in each differential pair each comprises a source coupled to its respective common node.

5. The amplifier of claim 4 wherein the first and second transistors in each of the differential pairs each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

6. The amplifier of claim 3 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form the differential output.

7. The amplifier of claim 1 wherein the current switch comprises a transistor.

8 The amplifier of claim 7 wherein the transistor comprises a field effect transistor.

9. The amplifier of claim 8 wherein the transistor comprises a drain coupled to its respective current control input.

10. The amplifier of claim 1 wherein the current switch comprises a current source having a switch control input.

11. The amplifier of claim 10 further comprising a bias circuit coupled to the switch control input.

12. The amplifier of claim 11 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

13. The amplifier of claim 12 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

14. The amplifier of claim 13 wherein the summer comprises a cascode current mirror.

15. The amplifier of claim 12 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

16. The amplifier of claim 1 further comprising a matching circuit coupled to the common differential output.

17. The amplifier of claim 16 wherein the matching circuit converts a differential current from the common differential output to a single-ended current.

18. The amplifier of claim 16 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the differential pairs is switched in or out of the amplifier.

19. The amplifier of claim 16 wherein the common differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

20. The amplifier of claim 1 wherein the differential pairs are further coupled together through a common differential input, the amplifier further comprising an input stage coupled to the common differential input.

21. The amplifier of claim 1 further comprising a plurality of current switches each coupled to the current control input for a different one of the differential pairs to selectively switch its respective differential pair in or out of the amplifier.

22. An amplifier, comprising:

a plurality of amplifying stages each having first and second transistors, the first and second transistors each having first, second and third nodes, the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output, the second nodes of the first transistors being coupled together and the second nodes of the second transistors being coupled together to form a differential input, and the third node of each of the first transistors being coupled to the third node of its respective second transistor to form a current control input for each of the amplifying stages; and

a current switch coupled to the current control input of one the amplifying stage to switch said one of the amplifying stages in or out of the amplifier.

23. The amplifier of claim 22 wherein the transistors each comprises a field effect transistor.

24. The amplifier of claim 23 wherein the third nodes each comprises a source.

25. The amplifier of claim 24 wherein the second nodes each comprises a gate.

26. The amplifier of claim 23 wherein the first nodes each comprises a drain.

27. The amplifier of claim 22 wherein the current switch comprises a transistor.

28. The amplifier of claim 27 wherein the transistor comprises a field effect transistor.

29. The amplifier of claim 28 wherein the transistor comprises a drain coupled to its respective current control input.

30. The amplifier of claim 22 wherein the current switch comprises a current source having a switch control input.

31. The amplifier of claim 30 further comprising a bias circuit coupled to the switch control input.

32. The amplifier of claim 31 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied the switch control input.

33. The amplifier of claim 32 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

34. The amplifier of claim 33 wherein the summer comprises a cascode current mirror.

35. The amplifier of claim 34 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

36. The amplifier of claim 22 further comprising a matching circuit coupled to the differential output.

37. The amplifier of claim 36 wherein the matching circuit converts a differential current from the differential output to a single-ended current.

38. The amplifier of claim 36 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the amplifying stages is switched in or out of the circuit.

39. The amplifier of claim 36 wherein the common differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

40. The amplifier of claim 22 further comprising an input stage coupled to the differential input.

41. The amplifier of claim 22 further comprising a plurality of current switches each coupled the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

42. An amplifier, comprising:

a plurality of amplifying stages coupled together, each of the amplifying stages having a current control input; and

a current switch coupled to the current control input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit.

43. The amplifier of claim 42 wherein the amplifying stages each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

44. The amplifier of claim 43 wherein the transistors each comprises a field effect transistor.

45. The amplifier of claim 44 wherein the first and second transistors in each amplifying stage comprises a source coupled to its respective common node.

46. The amplifier of claim 45 wherein the first and second transistors in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

47. The amplifier of claim 44 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

48. The amplifier of claim 42 wherein the current switch comprises a transistor.

49 The amplifier of claim 48 wherein the transistor comprises a field effect transistor.

50. The amplifier of claim 49 wherein the transistor comprises a drain coupled to its respective current control input.

51. The amplifier of claim 42 wherein the current switch comprises a current source having a switch control input.

52. The amplifier of claim 51 further comprising a bias circuit coupled to the switch control inputs.

53. The amplifier of claim 52 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

54. The amplifier of claim 53 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

55. The amplifier of claim 54 wherein the summer comprises a cascode current mirror.

56. The amplifier of claim 53 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

57. The amplifier of claim 42 further comprising a matching circuit coupled to the differential output.

58. The amplifier of claim 57 wherein the matching circuit converts a differential current from the differential output to a single-ended current.

59. The amplifier of claim 57 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the amplifying stages is switched in or out of the circuit.

60. The amplifier of claim 57 wherein the differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

61. The amplifier of claim 42 wherein the amplifying stages are coupled together to form a differential input, the amplifier further comprising an input stage coupled to the differential input.

62. The amplifier of claim 22 further comprising a plurality of current switches each coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

63. An amplifier comprising a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level.

64. The amplifier of claim 63 wherein the amplifier comprises CMOS.

65. The amplifier of claim 63 further comprising a plurality of amplifying stages coupled together, each of the amplifying stages having a current control input, and a plurality of current switches to digitally program the power level of the amplifier, the current switches each being coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

66. The amplifier of claim 65 wherein the amplifying stages each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

67. The amplifier of claim 66 wherein the transistors each comprises a field effect transistor.

68. The amplifier of claim 67 wherein the first and second transistors in each amplifying stage comprises a source coupled to its respective common node.

69. The amplifier of claim 68 wherein the first and second transistors in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

70. The amplifier of claim 67 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

71. The amplifier of claim 65 wherein the current switches each comprises a transistor.

72 The amplifier of claim 71 wherein the transistors each comprises a field effect transistor.

73. The amplifier of claim 72 wherein the transistors each comprises a drain coupled to its respective current control input.

74. The amplifier of claim 65 wherein the current switches each comprises a current source having a switch control input.

75. The amplifier of claim 74 further comprising a plurality of bias circuits each coupled to a different one of the switch control inputs.

76. The amplifier of claim 75 wherein the bias circuits each generates a bias current which is substantially independent of temperature, the bias current being applied to its respective switch control input.

77. The amplifier of claim 76 wherein the bias circuits each comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the its respective switch control input.

78. The amplifier of claim 77 wherein the summer comprises a cascode current mirror.

79. The amplifier of claim 76 wherein the current sources each comprises a field effect transistor having a gate comprising the switch control input.

80. An amplifier, comprising:

a plurality of amplifying stages coupled together;

switching means for switching one of the amplifying stages in or out of the amplifier to program power of the amplifier; and

matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power.

81. The amplifier of claim 80 wherein each of said one of the amplifying stage comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

82. The amplifier of claim 81 wherein the transistors each comprises a field effect transistor.

83. The amplifier of claim 82 wherein the first and second transistors each comprises a source coupled to its respective common node.

84. The amplifier of claim 83 wherein the amplifying stages each comprises first and second field effect transistors each having a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

85. The amplifier of claim 82 wherein the amplifying stages each comprises first and second field effect transistors each having a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

86. The amplifier of claim 80 wherein the switching means comprises a transistor.

87 The amplifier of claim 86 wherein the transistor comprises a field effect transistor.

88. The amplifier of claim 87 wherein the transistor comprises a drain coupled to said one of the amplifying stages.

89. The amplifier of claim 80 wherein the switching means comprises a current source having a switch control input.

90. The amplifier of claim 89 further comprising a bias circuit coupled to the switch control input.

91. The amplifier of claim 90 wherein the bias circuit comprises means for generating a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

92. The amplifier of claim 90 wherein the bias circuit comprises means for generating a first bias current exhibiting a positive temperature coefficient, means for generating a second bias current exhibiting a negative temperature coefficient, and means

for summing the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

93. The amplifier of claim 92 wherein the summer comprises a cascode current mirror.

94. The amplifier of claim 80 wherein the matching means comprises means for converting a differential current generated by the amplifier stage to a single-ended current, the single-ended current being coupled to the amplifier output.

95. The amplifier of claim, 80 wherein the amplifying stages comprises a differential output having first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled to the amplifier output.